Cellular Neural Networks for Associative Memories

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I. INTRODUCTION AND PRELIMINARIES

In this letter, we announce a synthesis procedure for designing nonsymmetric cellular neural networks (CNN) with a predetermined local interconnection structure that will store a set of desired bipolar vectors as memory points.

Cellular neural networks, introduced by Chua and Yang [2], are among the easiest to implement via VLSI and have found applications in image processing and pattern classification [3], [6]. However, the lack of a systematic synthesis procedure for CNN has restricted their applications in some cases, for example, in the area of associative memories.

We consider neural networks described by equations of the form

\[ \frac{dx}{dt} = -Ax + T \text{sat}(x) + I \]

(1)

where \( x \in R^n \), \( y \in D^n \), \( T = [T_{ij}] \in R^{n \times n} \), \( I = (I_1, \ldots, I_n)^T \in R^n \), \( \text{sat}(x) = [\text{sat}(x_1), \ldots, \text{sat}(x_n)]^T \), and \( \text{sat}(x_i) = 1 \) if \( x_i > 1 \), \( x_i = 1 \) if \( -1 < x_i \leq 1 \), and \( \text{sat}(x_i) = -1 \) if \( x_i < -1 \). We assume that the initial states of (1) satisfy \( |x_i(0)| \leq 1 \) for \( i = 1, \ldots, n \).

For ease of presentation, let \( \lambda = 1 \). Then for each \( x \in B^n \), we define \( \text{C}(\alpha) = \{ x \in R^n : x_i = 1 \text{ or } -1, i = \ldots, n \} \), where \( \alpha = \{0, 1\} \) is a finite state space, and each \( x \in C(\alpha) \), the first equation of (1) can be written as

\[ \dot{x} = -x + T \alpha + I. \]

(2)

System (2) has a unique equilibrium at \( x_e = T \alpha + I \), and \( x_e \) is in \( C(\alpha) \) by assumption. Clearly, this equilibrium is also asymptotically stable, since system (2) has all its \( n \) eigenvalues at \(-1\).

II. SYNTHESIS PROCEDURE FOR CNN’S

We first introduce some notation which shows how to relate (1) to the nonsymmetric CNN model [2]. The basic unit in CNN’s is called a cell. In a two-dimensional CNN, there are \( M \times N \) such cells arranged in an array of \( M \) rows and \( N \) columns. The cell in the \( i \)th row and the \( j \)th column is denoted by \( C(i, j) \), and the \( r \)-neighborhood \( N_r(i, j) \) of cell \( C(i, j) \) for a positive integer \( r \) is defined by

\[ N_r(i, j) = \{ C(k, l) : \max \{ |k - i|, |l - j| \} \leq r \}, \]

\[ 1 \leq k \leq M, 1 \leq l \leq N \}. \]

For every positive integer \( r \), we define a matrix \( Q = [Q_{ij}] \in R^{MN \times MN} \) as

\[ Q_{ij} = 1 \text{ if } C(i, j) \in N_r(i, j), \]

and

\[ Q_{ij} = 0 \text{ otherwise. } \]

(3)

We let \( S = Q = [S_{ij}] \in R^{MN \times MN} \), where \( m = MN \). Let \( W[S = h_{ij}] \in R^{MN \times MN} \) denote the restriction of \( W = [W_{ij}] \in R^{MN \times MN} \) on \( S \), i.e., \( h_{ij} = W_{ij} \) if \( S_{ij} = 1 \) and \( h_{ij} = 0 \) otherwise. With this notation, we see that in order for (1) to be equivalent to the nonsymmetric cellular neural network model given in [1], [2], we need \( T = T[S] \).

We now consider the following problem.

Synthesis Problem (S): Given positive integers \( r, m, M, N \), and vectors \( \alpha^1, \ldots, \alpha^m \in B^n \), choose \( T, I \) in such a manner that \( T = T[S] \) and \( \alpha^1, \ldots, \alpha^m \) are reachable memory vectors of system (1), where \( S = Q \) and \( Q \) is defined in (3).

The solution for the above synthesis problem, given in the following, is a generalization of the synthesis procedures developed in [4] and [7].

CNN Design Procedure (D): Suppose that we are given positive integers \( r, m, M, N \), and vectors \( \alpha^1, \ldots, \alpha^m \in B^n \) which are to be stored as reachable memory vectors for cellular neural network (1). We proceed as follows.

1. Compute the matrix \( Q \) as in (3) and denote \( S = Q = [S_{ij}] \in R^{MN \times MN} \).

2. Choose a real number \( k > 1 \) and \( m \) vectors \( \beta^1, \ldots, \beta^m \), such that \( \beta^i = k \alpha^i \).

3. Compute the \( n \times (m - 1) \) matrices \( Y = [y^1, \ldots, y^{m-1}] = [\alpha^1 - \alpha^m, \ldots, \alpha^{m-1} - \alpha^m, \alpha^1 - \alpha^m, \ldots, \alpha^{m-1} - \alpha^m] \), and \( Z = [z^1, \ldots, z^{m-1}] = [\beta^1 - \beta^2, \ldots, \beta^{m-1} - \beta^m] \). We define \( y_i = (y^1_i, \ldots, y^{m-1}_i)^T \) and \( z_i = (z^1_i, \ldots, z^{m-1}_i)^T \) for \( i = 1, \ldots, m - 1 \).

4. Denote the \( i \)-th row of the index matrix \( S \) by \( S_i = (S_{i1}, \ldots, S_{in}) \). For each \( i = 1, \ldots, n \), construct two sets \( M_i \) and \( N_i \), such that \( M_i \cup N_i = \{ i = 1, \ldots, n \}, M_i \cap N_i = \phi \), and \( S_{ij} = 1 \) if \( j \in M_i \), \( S_{ij} = 0 \) if \( j \in N_i \). Let \( M_i = \{i(1), \ldots, i(m_i)\} \), where \( m_i = \sum_{j=1}^{n} S_{ij} \), and \( s_i(k) < s_i(l) \) if \( 1 \leq k < l \leq m_i \). (Note that \( m_i \) is the number of nonzero elements in the \( i \)-th row of matrix \( S \).)

5. For \( i = 1, \ldots, n \), and \( l = 1, \ldots, m - 1 \), let \( y_{il} = (y^1_{i(1)}, \ldots, y^{m-1}_{i(m_i)})^{T} \).

6. For \( i = 1, \ldots, n \), compute the \( m \times (m - 1) \) matrices \( Y_1 = [y^1_i, \ldots, y^{m-1}_i] \), and the \( 1 \times (m - 1) \) vectors \( Z_1 = [z^1_i, \ldots, z^{m-1}_i] \).

7. For \( i = 1, \ldots, n \), perform a singular value decompositions of \( Y_i \), and obtain

\[ Y_i = [U_{i1} \mid U_{i2}] \begin{bmatrix} D_i & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_{i1}^T \\ V_{i2} \end{bmatrix} \]

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where $D_i \in \mathbb{R}^{n_i \times p_i}$ is a diagonal matrix with the nonzero singular values of $Y_i$ on its diagonal, and $p_i = \text{rank}(Y_i)$.

8. Compute for $i = 1, \cdots, n$, $G_i = [G_{i1}, \cdots, G_{im_i}] = Z_i V_i D_i^{-1} U_i^T + W_i U_i^T$, where $W_i$ is an arbitrary $1 \times (m_i - p_i)$ real vector.

9. The matrix $T = [T_{ij}]$ is computed as follows:

$$T_{ij} = 0 \text{ if } S_{ij} = 0 \quad \text{ and } T_{ij} = G_{ik} \text{ if } S_{ij} \neq 0$$
and if $j = \sigma_i(k)$. (4)

10. The bias vector $I = (I_1, \cdots, I_n)^T$ is computed by $I_i = \beta_i - T_i \alpha_i$ for $i = 1, \cdots, n$, where $T_i$ is the $i$th row of the matrix $T$. Then $\alpha_1, \cdots, \alpha_m$ will be stored as memory vectors for the system of form (1) with $T$ and $I$ determined above. The states $\beta_1, \cdots, \beta_m$ will become asymptotically stable equilibrium points of the synthesized system.

The validity of the above procedure is based on the following result.

**Theorem 1:** 1) The above design procedure guarantees that $T = T(S, 2)$. The CNN design procedure (D) can be applied to any desired memory patterns $\alpha_1, \cdots, \alpha_m \in B^n$. 3) The CNN design procedure (D) guarantees that every $\alpha_i$ is stored as a reachable memory vector of system (1).

**Proof:** Part 1) is clear from (4). A proof for part 2) is given in [5]. Part 3) can be proved from Lemma 1 by taking $k > 1$ small in step 2).

**Remark 1:** If we wish that the above design procedure results in a system of form (1) with $I = 0$, we can modify the CNN design procedure (D) as follows. a) In step 3), take $Y = [\alpha_1^*, \cdots, \alpha_m^*]$ and $Z = [\beta_1^*, \cdots, \beta_m^*]$; b) In step 10), take $I = 0$. Then all conclusions will remain unchanged. In particular, each $-\beta_i$ and $-\alpha_i$, $i = 1, \cdots, m$, will also be an asymptotically stable equilibrium point and a memory vector, respectively, of the synthesized system (1). ■

Our next result concerns the modified design procedure. A proof will be given in [5].

**Theorem 2:** Suppose that $\alpha_1, \cdots, \alpha_m$ are reachable memory vectors obtained by the modified design procedure. Suppose that $\eta$ is a linear combination of $\alpha_1, \cdots, \alpha_m$ and $\eta \in B^n$. Then, the modified CNN design procedure (D) as discussed in Remark 1 will guarantee that $\eta$ is a reachable memory vector of the synthesized system. ■

Note that the CNN design procedure (D) and its modified version will generally result in a CNN with nonsymmetric (or nonreciprocal [1]) interconnections.

### III. AN EXAMPLE

We next present a specific case to demonstrate the applicability of our results.

**Example:** We consider 25 desired memory patterns $\alpha_1^*, \cdots, \alpha_25^*$ as shown in Fig. 1. Each pattern represents a basic module which is used in constructing Chinese characters and corresponds to a vector in $\mathbb{R}^{n_i}$ with each vector component varying from $-1$ to $1$ determined by the gray level (cf., Fig. 2) in the corresponding box. If the gray level in a box is white (black), the value of the corresponding component is $-1$ (1).

We wish to synthesize a CNN (1) with $n = 81$ ($M = N = 9$) and $r = 3$, which will "remember" certain Chinese characters. Many Chinese characters can be separated into two modules. In particular, the patterns given in Fig. 1 can be used to generate at least 50 commonly used Chinese characters. To demonstrate this, we add one more vector, $\alpha_{26}^*$, with every entry equal to 1, to the set of desired memory patterns. By adding $\alpha_{26}^*$ to the set of desired memory patterns, we can generate desired combinations for Chinese characters made up of the basic modules given in Fig. 1. For instance, the Chinese character corresponding to $\alpha_6^*$ means "sun" and the Chinese character corresponding to $\alpha_1^* \alpha_2^*$ means "moon." A new Chinese character can be generated as $\alpha_3^* = \alpha_6^* + \alpha_1^* \alpha_2^*$, which means "bright." Using the modified CNN design procedure (D) as discussed in Remark 1, we only need to synthesize.
a system (1) with interconnections restricted to local neighborhoods of radius \( r \) by employing these basic patterns. The resulting system will automatically "remember" all possible combinations of the basic modules, including the 50 commonly used Chinese characters mentioned above (by Theorem 2).

In the modified CNN design procedure, taking \( k = 2 \) in step 2) and \( W_i = -10 \times O_{max} \times U_{c2} \) in step 8), where \( O_{max} = (1, \ldots, 1) \in R^{1 \times m} \), and \( m_i = \sum_{j=1}^{n} S_{ij} \), we design a CNN of form (1) with neighborhood radius \( r = 3 \) which stores \( \alpha_1, \ldots, \alpha_{25} \) as memory vectors. This system has 2601 total interconnections, while using a fully interconnected neural network with \( n = 81 \), we require a total of 6561 interconnections. For the present example, by using a CNN, we have reduced the total number of required interconnections to less than 40%.

One of the typical evolution results for \( \alpha_{27} = \alpha_6 + \alpha_9 + \alpha_{30} \) is depicted in Fig. 5. The noisy initial pattern shown in the upper left corner of Fig. 3 is generated by adding to \( \alpha_{27} \) zero-mean Gaussian noise with a standard deviation \( \text{SD} = 1 \). The evolution continues from left to right in each row and from the top row to the bottom row. The key pattern \( \alpha_{37} \) is recovered in 24 steps with step size \( \text{step} = 0.227 \) in a digital simulation of (1), using MATLAB on a Sun SPARC Station.

Simulation results also show that all the vectors corresponding to the aforementioned 50 commonly used Chinese characters are reachable memory vectors of the synthesized CNN.

REFERENCES


Reply to "Comments on 'Linearization Techniques for Nth-Order Sensor Models in MOS VLSI Technology'"1

Mohammed Ismail

Contrary to common practice, the above comments1 were not made available to us for reply prior to publication. We would like to think that this was an oversight. In the following, we provide our reply.

The four-transistor MOS transistor presented in [1] provides the most general description of the circuit concept in question. A nonlinearity cancellation condition relating the gate voltages of the four transistors was developed together with general conditions on transistors drain-source voltages for proper triode region operation. We then show that the independent works of Song [2], Rubin [3], Ryan-Haigh [4], and the author of the comments are special cases of the general description provided in [1]. Our general approach was adopted in the text by Unbehauen and Cichocki [5] to describe the circuit and its special cases. This approach shows that while MOS circuits may look topologically identical, they could exhibit extremely different behaviors under different operating conditions. More recently [6], we show that complete nonlinearity cancellation in the circuit occurs when all four transistors operate in saturation or when the cross-coupled pair operates in triode (saturation) while the other pair operates in saturation (triode). In all these cases, the circuit topology is the same, which leads us to argue that the origin of the circuit really goes back to the four-transistor chopper multiplier [7] which is topologically identical (see [7, figs. 6 and 9]) to the circuit in question, and in which the four transistors, when on, operate in both triode and saturation. Our understanding and recognition of the circuit concept as such and of the extent to which it can be used has led to our development of the first single op-amp all-MOS multiplier/divider (Elec. Lett., pp. 1550–1551, 1989) which is widely acknowledged by many researchers and is now documented in several texts (e.g., [5], [8]). Furthermore, a United States patent was recently issued to us [9] for a multiplier/divider circuit that is even simpler (uses a single op-amp and half the number of transistors). A third multiplier/divider circuit which also uses a lower number of transistors was reported recently (Ismail et al., ISCAS '93). The latter circuit is based on a two-transistor MOS transistor (first reported by Ismail and Prigeon, Proc. ISCAS, pp. 1655–1668, 1988) which achieves complete nonlinearity cancellation and has the same transconductance of the four-transistor circuit. All of these multiplier/dividers were extended to the multi-input case for system level applications, and operating signal conditions (which are different from those in the four-transistor circuit) were established (see, e.g., reference [14] in the comments).

The Double-MOSFET method (first developed in print by Ismail et al., IJSSC, Feb. 1988) that was raised in the above comment1 is a design methodology relating the four-transistor circuit to a pair of voltage-controlled floating resistors and as such provides a systematic way to convert active-RC prototypes to MOSFET-C counterparts. Furthermore, it establishes necessary topological conditions that must

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