Express Letters

Cellular Neural Networks for Associative Memories

Derong Liu and Anthony N. Michel

I. Introduction and Preliminaries

In this letter, we announce a synthesis procedure for designing *nonsymmetric* cellular neural networks (CNN) with a predetermined local interconnection structure that will store a set of desired bipolar vectors as memory points.

Cellular neural networks, introduced by Chua and Yang [2], are among the easiest to implement via VLSI and have found applications in image processing and pattern classification [3], [6]. However, the lack of a (systematic) synthesis procedure for CNN has restricted their applications in some cases, for example, in the area of associative memories.

We consider neural networks described by equations of the form

$$\begin{cases} \frac{dx}{dt} = -Ax + T\,\mathrm{sat}(x) + I \\ y = \mathrm{sat}(x) \end{cases} \tag{1}$$

where $x \in R^n$, $y \in D^n \triangleq \{x \in R^n: -1 \le x_i \le 1, i = 1, \cdots, n\}$, $A = \mathrm{diag}[\lambda, \cdots, \lambda]$ with $\lambda > 0$, $T = [T_{ij}] \in R^{n \times n}$, $I = (I_1, \cdots, I_n)^T \in R^n$, $\mathrm{sat}(x) = [\mathrm{sat}(x_1), \cdots, \mathrm{sat}(x_n)]^T$, and $\mathrm{sat}(x_i) = 1$ if $x_i > 1$, $\mathrm{sat}(x_i) = x_i$ if $-1 \le x_i \le 1$, and $\mathrm{sat}(x_i) = -1$ if $x_i < -1$. We assume that the initial states of (1) satisfy $|x_i(0)| \le 1$ for $i = 1, \cdots, n$.

For ease of presentation, we let $\lambda = 1$. For each $\alpha \in B^n \triangleq \{x \in R^n: x_i = 1 \text{ or } -1, i = 1, \cdots, n\}$, we define $C(\alpha) = \{x \in R^n: x_i\alpha_i > 1, i = 1, \cdots, n\}$.

We give next a result which is preliminary to our synthesis procedure.

Lemma 1: Suppose $\alpha \in B^n$. If $\beta = T\alpha + I \in C(\alpha)$, then β is an asymptotically stable equilibrium point of (1).

Proof: Since $\alpha_i = \pm 1$ for all i, we see that $\mathrm{sat}(x) = \alpha$ for all $x \in C(\alpha)$. For $x \in C(\alpha)$, the first equation of (1) can be written as

$$\dot{x} = -x + T\alpha + I. \tag{2}$$

System (2) has a unique equilibrium at $x_e = T\alpha + I$, and $x_e = \beta \in C(\alpha)$ by assumption. Clearly, this equilibrium is also asymptotically stable, since system (2) has all its n eigenvalues at -1. ■

If $\xi \in R^n$ is an asymptotically stable equilibrium point of (1), then $y_\xi = \mathrm{sat}(\xi)$ is said to be a memory vector of (1). A memory vector y_ξ of (1) is said to be reachable, if there exists a neighborhood V of y_ξ, such that for any $x(0) \in V \cap D^n \neq \phi$, the output vector $y(t)$ of (1) tends to y_ξ asymptotically as $t \to \infty$.

II. Synthesis Procedure for CNN's

We first introduce some notation which shows how to relate (1) to the *nonsymmetric* CNN model [2]. The basic unit in CNN's is called a cell. In a two-dimensional CNN, there are $M \times N$ such cells arranged in an array of M rows and N columns. The cell in the ith row and the jth column is denoted by $C(i, j)$, and the r-neighborhood $N_r(i, j)$ of the cell $C(i, j)$ for a positive integer r is defined by

$$N_r(i, j) \triangleq \{C(k, l): \max\{|k - i|, |l - j|\} \le r, \\ 1 \le k \le M, 1 \le l \le N\}.$$

For every given positive integer r, we define a matrix $Q = [Q_{ij,\,kl}] \in R^{MN \times MN}$ as

$$Q_{ij,\,kl} = 1 \text{ if } C(k, l) \in N_r(i, j), \quad \text{and} \\ Q_{ij,\,kl} = 0 \quad \text{otherwise.} \tag{3}$$

We let $S = Q = [S_{ij}] \in R^{n \times n}$, where $n = MN$. Let $W|S = [h_{ij}] \in R^{n \times n}$ denote the restriction of $W = [W_{ij}] \in R^{n \times n}$ on S, i.e., $h_{ij} = W_{ij}$ if $S_{ij} = 1$ and $h_{ij} = 0$ otherwise. With this notation, we see that in order for (1) to be equivalent to the nonsymmetric cellular neural network model given in [1], [2], we need $T = T|S$.

We now consider the following problem.

Synthesis Problem (S): Given positive integers r, n, M, and N with $n = M \times N$, and m vectors $\alpha^1, \cdots, \alpha^m$ in B^n, choose $\{T, I\}$ in such a manner that $T = T|S$ and $\alpha^1, \cdots, \alpha^m$ are reachable memory vectors of system (1), where $S = Q$ and Q is defined in (3). ■

The solution for the above synthesis problem, given in the following, is a generalization of the synthesis procedures developed in [4] and [7].

CNN Design Procedure (D): Suppose that we are given positive integers r, n, M, and N with $n = M \times N$, and m vectors $\alpha^1, \cdots, \alpha^m$ in B^n which are to be stored as reachable memory vectors for cellular neural network (1). We proceed as follows.

1. Compute the matrix Q as in (3) and denote $S = Q = [S_{ij}] \in R^{n \times n}$.
2. Choose a real number $k > 1$ and m vectors $\beta^1, \cdots, \beta^m$, such that $\beta^i = k\alpha^i$.
3. Compute the $n \times (m - 1)$ matrices $Y = [y^1, \cdots, y^{m-1}] = [\alpha^1 - \alpha^m, \cdots, \alpha^{m-1} - \alpha^m]$, and $Z = [z^1, \cdots, z^{m-1}] = [\beta^1 - \beta^m, \cdots, \beta^{m-1} - \beta^m]$. We denote $y^i = (y_1^i, \cdots, y_n^i)^T$ and $z^i = (z_1^i, \cdots, z_n^i)^T$ for $i = 1, \cdots, m - 1$.
4. Denote the ith row of the index matrix S as $S_i = (S_{i1}, \cdots, S_{in})$. For each $i = 1, \cdots, n$, construct two sets M_i and N_i, such that $M_i \cup N_i = \{i = 1, \cdots, n\}$, $M_i \cap N_i = \phi$, and $S_{ij} = 1$ if $j \in M_i$, $S_{ij} = 0$ if $j \in N_i$. Let $M_i = \{\alpha_i(1), \cdots, \sigma_i(m_i)\}$, where $m_i = \sum_{j=1}^n S_{ij}$, and $\sigma_i(k) < \sigma_i(l)$ if $1 \le k < l \le m_i$. (Note that m_i is the number of nonzero elements in the ith row of matrix S.)
5. For $i = 1, \cdots, n$, and $l = 1, \cdots, m - 1$, let $y^l_{Ii} = (y^l_{\sigma(1)}, \cdots, y^l_{\sigma(m_i)})^T$.
6. For $i = 1, \cdots, n$, compute the $m_i \times (m - 1)$ matrices $Y_i = [y^1_{Ii}, \cdots, y^{m-1}_{Ii}]$, and the $1 \times (m - 1)$ vectors $Z_i = [z^1_i, \cdots, z^{m-1}_i]$.
7. For $i = 1, \cdots, n$, perform a singular value decompositions of Y_i, and obtain

$$Y_i = [U_{i1} \mid U_{i2}] \left[\begin{array}{c|c} D_i & 0 \\ \hline 0 & 0 \end{array}\right] \left[\begin{array}{c} V_{i1}^T \\ \hline V_{i2}^T \end{array}\right]$$

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where $D_i \in R^{p_i \times p_i}$ is a diagonal matrix with the nonzero singular values of Y_i on its diagonal, and $p_i = \text{rank}(Y_i)$.

8. Compute for $i = 1,\cdots,n$, $G_i = [G_{i1},\cdots,G_{im_i}] = Z_i V_{i1} D_i^{-1} U_{i1}^T + W_i U_{i2}^T$, where W_i is an arbitrary $1 \times (m_i - p_i)$ real vector.
9. The matrix $T = [T_{ij}]$ is computed as follows:

$$T_{ij} = 0 \text{ if } S_{ij} = 0 \qquad \text{and } T_{ij} = G_{ik} \text{ if } S_{ij} \neq 0 \text{ and if } j = \sigma_i(k). \quad (4)$$

10. The bias vector $I = (I_1,\cdots,I_n)^T$ is computed by $I_i = \beta_i^m - T_i\alpha^m$, for $i = 1,\cdots,n$, where T_i is the ith row of the matrix T. Then $\alpha^1,\cdots,\alpha^m$ will be stored as memory vectors for the system of form (1) with T and I determined above. The states $\beta^1,\cdots,\beta^m$ will become asymptotically stable equilibrium points of the synthesized system. ∎

The validity of the above procedure is based on the following results.

Theorem 1: 1) The above design procedure guarantees that $T = T|S$. 2) The CNN design procedure (D) can be applied to any desired memory patterns $\alpha^1,\cdots,\alpha^m \in B^n$. 3) The CNN design procedure (D) guarantees that every α^i is stored as a reachable memory vector of system (1).

Proof: Part 1) is clear form (4). A proof for part 2) is given in [5]. Part 3) can be proved from Lemma 1 by taking $k > 1$ small in step 2). ∎

Remark 1: If we wish that the above design procedure results in a system of form (1) with $I = 0$, we can modify the CNN design procedure (D) as follows. a) In step 3), take $Y = [\alpha^1,\cdots,\alpha^m]$ and $Z = [\beta^1,\cdots,\beta^m]$. b) In step 10), take $I = 0$. Then all conclusions will remain unchanged. In particular, each $-\beta^i$ and $-\alpha^i$, $i = 1,\ldots,m$, will also be an asymptotically stable equilibrium point and a memory vector, respectively, of the synthesized system (1). ∎

Our next result concerns the modified design procedure. A proof will be given in [5].

Theorem 2: Suppose that $\alpha^1,\cdots,\alpha^m$ are reachable memory vectors obtained by the modified design procedure. Suppose that η is a linear combination of $\alpha^1,\cdots,\alpha^m$ and $\eta \in B^n$. Then, the modified CNN design procedure (D) as discussed in Remark 1 will guarantee that η is a reachable memory vector of the synthesized system. ∎

Note that the CNN design procedure (D) and its modified version will generally result in a CNN with nonsymmetric (or nonreciprocal [1]) interconnections.

III. An Example

We next present a specific case to demonstrate the applicability of our results.

Example: We consider 25 desired memory patterns $\alpha^1,\cdots,\alpha^{25}$ as shown in Fig. 1. Each pattern represents a basic module which is used in constructing Chinese characters and corresponds to a vector in R^{81} with each vector component varying from -1 to 1 determined by the gray level (cf., Fig. 2) in the corresponding box. If the gray level in a box is white (black), the value of the corresponding component is -1 (1).

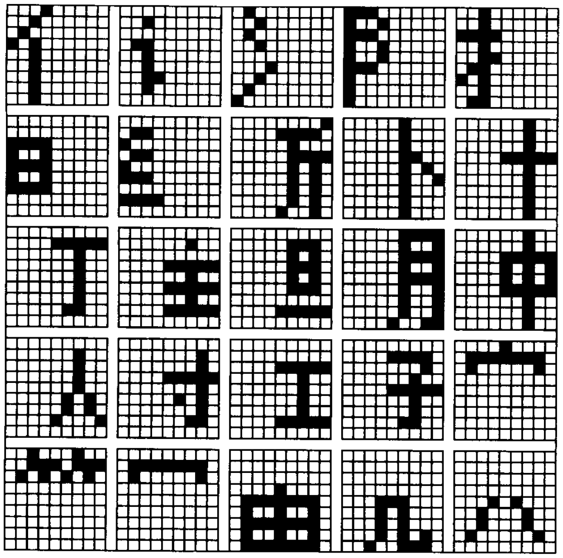

Fig. 1. The 25 desired memory patterns used in the example.

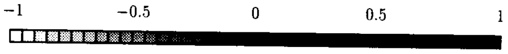

Fig. 2. Gray levels.

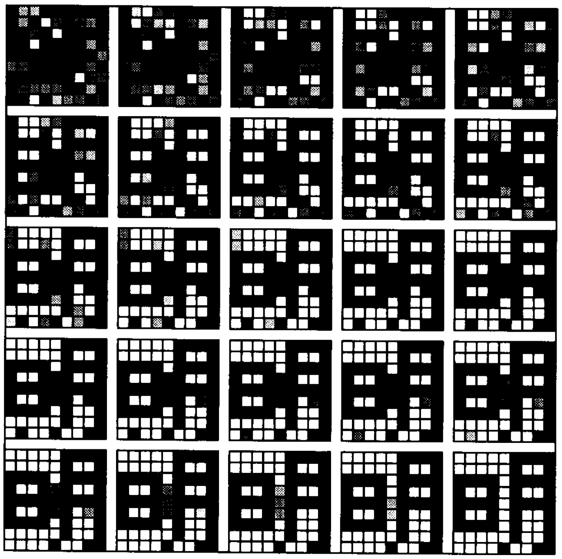

Fig. 3. A typical evolution of the Chinese character composed of patterns 6 and 14 in Fig. 1.

We wish to synthesize a CNN (1) with $n = 81$ ($M = N = 9$) and $r = 3$, which will "remember" certain Chinese characters. Many Chinese characters can be separated into two modules. In particular, the patterns given in Fig. 1 can be used to generate at least 50 commonly used Chinese characters. To demonstrate this, we add one more vector, α^{26}, with every entry equal to 1, to the set of desired memory patterns. By adding α^{26} to the set of desired memory patterns, we can generate desired combinations for Chinese characters made up of the basic modules given in Fig. 1. For instance, the Chinese character corresponding to α^6 means "sun" and the Chinese character corresponding to α^{14} means "moon." A new Chinese character can be generated as $\alpha^{27} = \alpha^6 + \alpha^{14} + \alpha^{26}$, which means "bright." Using the modified CNN design procedure (D) as discussed in Remark 1, we only need to synthesize a system (1) with interconnections restricted to local neighborhoods of radius r by employing these basic patterns. The resulting system will automatically "remember" all possible combinations of the basic modules, including the 50 commonly used Chinese characters mentioned above (by Theorem 2).

In the modified CNN design procedure, taking $k = 2$ in step 2) and $W_i = -10 \times O_{m_i} \times U_{i2}$ in step 8), where $O_{m_i} = (1, \cdots, 1) \in R^{1 \times m_i}$ and $m_i = \sum_{j=1}^{n} S_{ij}$, we design a CNN of form (1) with neighborhood radius $r = 3$ which stores $\alpha^1, \cdots, \alpha^{26}$ as memory vectors. This system has 2601 total interconnections, while using a fully interconnected neural network with $n = 81$, we require a total of 6561 interconnections. For the present example, by using a CNN, we have reduced the total number of required interconnections to less than 40%.

One of the typical evolution results for $\alpha^{27} = \alpha^6 + \alpha^{14} + \alpha^{26}$ is depicted in Fig. 3. The noisy initial pattern shown in the upper left corner of Fig. 3 is generated by adding to α^{27} zero-mean Gaussian noise with a standard deviation SD = 1. The evolution continues from left to right in each row and from the top row to the bottom row. The key pattern α^{27} is recovered in 24 steps with step size $h = 0.227$ in a digital simulation of (1), using MATLAB on a Sun SPARC Station.

Simulation results also show that all the vectors corresponding to the aforementioned 50 commonly used Chinese characters are reachable memory vectors of the synthesized CNN. ■

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Reply to "Comments on 'Linearization Techniques for Nth-Order Sensor Models in MOS VLSI Technology' "[1]

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Contrary to common practice, the above comments[1] were not made available to us for reply prior to publication. We would like to think that this was an oversight. In the following, we provide our reply.

The four-transistor MOS transconductor presented in [1] provides the most general description of the circuit concept in question. A nonlinearity cancellation condition relating the gate voltages of the four transistors was developed together with general conditions on transistors drain-source voltages for proper triode region operation. We then show that the independent works of Song [2], Rubin [3], Ryan–Haigh [4], and the author of the comments are special cases of the general description provided in [1]. Our general approach was adopted in the text by Unbehauen and Cichocki [5] to describe the curcuit and its special cases. This approach shows that while MOS circuits may look topologically identical, they could exhibit extremely different behaviors under different operating conditions. More recently [6], we show that complete nonlinearity cancellation in the circuit occurs when all four transistors operate in saturation or when the cross-coupled pair operates in triode (saturation) while the other pair operates in saturation (triode). In all these cases, the circuit topology is the same, which leads us to argue that the *origin* of the circuit really goes back to the four-transistor chopper multiplier [7] which is topologically identical (see [7, figs. 6 and 9]) to the circuit in question, and in which the four transistors, when on, operate in both triode and saturation. Our understanding and recognition of the circuit concept as such and of the extent to which it can be used has led to our development of the first single op-amp all-MOS multiplier/divider (*Elec. Lett.*, pp. 1550–1551, 1989) which is very widely acknowledged by many researchers and is now documented in several texts (e.g., [5], [8]). Furthermore, a United States patent was recently issued to us [9] for a multiplier/divider circuit that is even simpler (uses a single op-amp and half the number of transistors). A third multiplier/divider circuit which also uses a lower number of transistors was reported recently (Ismail *et al.*, ISCAS '93). The latter circuit is based on a *two-transistor* MOS transconductor (first reported by Ismail and Prigeon, *Proc. ISCAS*, pp. 1655–1668, 1988) which achieves complete nonlinearity cancellation and has the same transconductance of the four-transistor circuit. All of these multiplier/dividers were extended to the multi-input case for system level applications, and operating signal conditions (which are different from those in the four-transistor circuit) were established (see, e.g., reference [14] in the comments).

The Double-MOSFET method (first developed in print by Ismail *et al.*, *IEEE JSSC*, Feb. 1988) that was raised in the above comment[1] is a *design methodology* relating the four-transistor circuit to a pair of voltage-controlled floating resistors and as such provides a systematic way to convert active-*RC* prototypes to MOSFET-C counterparts. Furthermore, it establishes necessary topological conditions that must

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